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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/526,009	02/25/2005	Akiyoshi Fujii	1248-0772PUS1	4652

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BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

EXAMINER	
KALAM, ABUL	

ART UNIT	PAPER NUMBER
2814	

NOTIFICATION DATE	DELIVERY MODE
04/30/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

Office Action Summary	Application No.	Applicant(s)	
	10/526,009	FUJII ET AL.	
	Examiner	Art Unit	
	Abul Kalam	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,9,10,26-29 and 34-38* is/are pending in the application.

4a) Of the above claim(s) *5,6,9 and 36-38* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,10,26-29,34 and 35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's election without traverse of Group IV, in the reply filed on January 23, 2009, is acknowledged.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. **Claims 1, 10 and 34** are rejected under 35 U.S.C. 102(a) as being anticipated by Wong et al. ("Amorphous silicon thin-film transistors and arrays fabricated by jet printing;" newly cited, hereinafter, Wong).

With respect to **claim 1**, Wong teaches a TFT array substrate, comprising:

a thin film transistor section **(FIG. 2)** in which a gate electrode **("Cr gate," FIG. 2b)** is formed on a substrate **("glass substrates," pg. 611, 1st ¶)**, and

a semiconductor layer **("a-Si layer," pg. 611, 1st ¶)**, formed by etching a semiconductor film after a mask material **("printed wax," pg. 611, 2nd ¶)** is dropped onto the semiconductor film **(FIGs. 2c-2d)**, is formed on the gate electrode **("Cr gate," FIGs. 2b-2c)** separated by a gate insulation layer **("Si_3N_4" layer formed over the gate, FIG. 2c)**, wherein the semiconductor layer **("a-Si," FIGs. 2c-2d)** having a shape formed by dropping a droplet **(pgs. 610-611)**.

With respect to claim 10, Wong teaches a flat panel display device including the TFT array substrate as set forth in the claim 1 **(pg. 610, 1st ¶)**. Regarding the limitation of a "liquid crystal display device," note that LCD devices comprising TFT array substrates are well known and conventional in the art. Furthermore, it has been held that a preamble is denied the effect of a limitation where the claim following the preamble is a self-contained description of the structure not depending for completeness upon the introductory clause. *Kropa v. Robie,* 88 USPQ 478 (CCPA 1951).

With respect to claim 34, Wong teaches an electronic device including the TFT array substrate as set forth in claim 1 **(pg. 610, 1st ¶)**. Regarding the limitation of an electronic device, it has been held that a preamble is denied the effect of a limitation where the claim following the preamble is a self-contained description of the structure not depending for completeness upon the introductory clause. *Kropa v. Robie,* 88 USPQ 478 (CCPA 1951).

Claim Rejections - 35 USC § 103

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. **Claims 2-4** are under 35 U.S.C. 103(a) as being unpatentable over Wong (cited above) in view of Kasahara et al. (US 6,822,701; hereinafter, Kasahara).

With respect to **claim 2**, Wong discloses all the limitations of claim, as set forth above in claim 1, including wherein the gate electrode **(Fig. 4, "gate")** in the thin film transistor section is a branch electrode which is branched out of a main line **(Fig. 4, "gate line")** of the gate electrode. However, Wong does not explicitly disclose wherein the branch electrode has an open end protruded from an area for the semiconductor layer.

However, Kasahara discloses a thin film transistor array **(Fig. 3)** wherein the gate electrode **(220)** in the TFT section **(24)** is branch electrode that has an open end **(Fig. 3, "e")** protruded from an area **(224A/224B)** of the semiconductor layer **(223, Fig. 2)**.

Regarding **claim 3,** Kasahara also teaches wherein the branch electrode is arranged so that a portion protruded **(Fig. 3, "e")** from the area for the semiconductor layer is smaller in width than a portion confined within the area **(224A/224B)** for the semiconductor layer.

Regarding **claim 4,** Kasahara also teaches wherein the thin film transistor section further includes a source electrode and a drain electrode **(221 and 222, Fig. 2)** on the semiconductor layer **(223)**, and a channel section is formed between the source and drain electrodes (a channel is inherently formed between the source and drain), and the portion of the branch electrode **(Fig. 3, "e")** protruded from the area for the semiconductor layer is formed in contact with one of the source and drain electrodes **(col. 14, lns. 31-40)**.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to combine the teaching of Kasahara and Wong, to form a thin film transistor array wherein the gate electrode comprises a branch electrode with a protruded portion, for the purpose of improving the process of repairing defective pixels in a display device **(col. 16, lns. 1-9)**.

4. **Claims 26-29 and 35** are under 35 U.S.C. 103(a) as being unpatentable over Yoo et al. (US 2002/0180898; newly cited, hereinafter, Yoo) in view of Wong (cited above).

With respect to **claim 26,** Yoo discloses a thin film transistor array substrate **(Figs. 6-8)**, comprising:

a thin film transistor array section **(Fig. 6, "TFT")** in which a gate electrode **(33, Fig. 7)** is formed on a substrate **(31, Fig. 7)**, and in which a semiconductor layer **(45 and 47; Fig. 7 and 8c)** and a conductor layer **(36a, Fig. 8c)** are formed on the gate electrode **(31)** separated by a gate insulation layer **(45, Fig. 8c)**;

wherein the conductor layer **(36; Figs. 8c)** is formed in contact with the semiconductor layer **(45 and 47, Fig. 8c)** and one of source and drain electrodes **(35, 37, Fig. 8c)** of the thin film transistor section, wherein the conductor layer **(36a, Fig. 8c)** and the semiconductor layer **(45 and 47)** having substantially the same shape **(Fig. 6 an 8c; ¶ [0056]-[0058], [0063]-[0066])**.

Thus, Yoo teaches all the limitations of the claim including wherein the conductor **(36a, Fig. 8c)** layer is part of the source and drain electrodes **(35 and 37; ¶ [0057])**.

However, Yoo does not teach wherein the semiconductor layer is formed by etching a semiconductor film after a mask material is dropped onto the semiconductor film; and wherein the conductor layer and the semiconductor layer have substantially the same shape in a portion where the conductor was formed by dropping a droplet.

Wong teaches a TFT array substrate **(FIGs. 2 and 4)** wherein the semiconductor layer **("a-Si layer," pg. 611, 1st ¶)** is formed by etching a semiconductor film after a mask material **("printed wax," pg. 611, 2nd ¶)** is dropped onto the semiconductor film **(FIGs. 2c-2d)**; wherein the source and drain electrodes **("source-drain metal," pg. 611, 1st ¶)** have a portion formed by dropping a droplet **(pg. 611, 3rd ¶)**, the source/drain electrodes **(Fig. 2f)** and the semiconductor layer **("a-Si," FIGs. 2c-2d)** having substantially the same shape in the portion formed by dropping a droplet **(pgs. 610-611: both the source/drain electrode and the semiconductor layer were formed dropping droplets (mask) onto the layers and then patterning the layers)**.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Wong into the invention of Yoo, thereby forming the conductor layer and the semiconductor layer using printed masks in place of conventional photolithography, because such a modification would have been considered a mere substitution of art recognized equivalents **(Yoo, pg. 610: abstract)** (MPEP 2144.06).

Regarding claims 27 and 28, Yoo discloses wherein the conductor layer is constituted of one of Mo, W, Cr, Ta, and Ti **(¶ [0057)** and the source and drain electrodes are made of Al **(¶ [0057])**.

Regarding claim 29, Yoo discloses a liquid crystal display device **(FIG. 6, ¶ [0056])** including the TFT array substrate as set forth in claim 26.

Regarding claim 35, Furusawa discloses an electronic device **(FIG. 6, ¶ [0056])** including the TFT array substrate as set forth in claim 26.

Response to Arguments

5. Applicant's arguments filed September 2, 2008, have been considered but are not persuasive.

Regarding claim 1, Applicant argues that "Wong does not teach the use of the drop shape from an inkjet in the creation of the semiconductor layer." The argument is not persuasive. Note that the claim 1 does not recite a "drop shape from an inkjet" but instead states "the formed semiconductor layer having a shape formed by dropping a droplet." Wang discloses that the mask layer, which is used to define the shape of the semiconductor active layer (pg. 611, 1st paragraph), is formed by dropping a droplet (pg. 610, paragraphs 5 and 6). Applicant's argument that Wang teaches rectangular semiconductor layers is not relevant, because the claim does not recite a specific shape for the semiconductor layer. Applicant's argument that the semiconductor layer is taught to be etched so as to be "self aligned to the Cr gate," and thus, "takes on the shape of the Cr gate," is not persuasive. Wong clearly states in 2nd paragraph on page

611, that the semiconductor active island is patterned by the wax-mask which was formed by dropping a droplet (pg. 610, paragraphs 5 and 6). Furthermore, it is the top nitride layer, not the semiconductor layer, which was formed using a self-aligned process (pg. 611, 3rd paragraph).

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abul Kalam whose telephone number is (571)272-8346. The examiner can normally be reached on Monday - Friday, 9 AM - 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/A. K./
Examiner, Art Unit 2814

/Phat X. Cao/
Primary Examiner, Art Unit 2814